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Attorney's Docket No.: 07977-204002 / US3480D1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Hisashi Ohtani
Serial No. : 09/389,393
Filed : September 3, 1999
Title : SEMICONDUCTOR DEVICE HAVING INSULATED GATE ELECTRODE

Art Unit : 2815
Examiner : Bradley Baumeister

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Commissioner for Patents
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REPLY TO ACTION OF NOVEMBER 17, 2004

In reply to the Final Office Action of November 17, 2004, Applicant submits the following remarks.

Claims 1, 44-48, and 55-84 are pending, of which claims 1 and 44-48 are independent. Claims 2-43 and 49-54 were previously cancelled.

In the Office Action, the drawings are not approved; specifically, FIG. 5 is objected to as not being disclosed in the specification as filed. Further, 1, 44-48, and 55-84 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement thereof.

In response, Applicant respectfully submits that the drawings, including FIG. 5, do not set forth new matter, and that claims 1, 44-48, and 55-84 are in full compliance with all requirements of 35 U.S.C. 112.

In particular, the Office Action asserts in paragraph 2, section a, that the specification, as filed, does not disclose for a bottom-gate TFT, "source/drain regions being laterally spaced from the first metal extending region." The Office Action further asserts in paragraph 5 that "Applicant has referenced the features of other drawings setting forth top gate embodiments, but has not pointed to any portion of the specification that supports the depiction or claiming of the noted features in a bottom gate embodiment."

In response, Applicant respectfully submits that the specification as filed clearly discloses a top-gate TFT having "source/drain regions being laterally spaced from the first metal extending region" (see, e.g., FIG. 2B or 2C, as well as page 9, lines 1-2, which discloses the regions 19 that